What we claim is:

1. A data processing circuit comprising:

a data processor which performs predetermined processing to data and outputs the data having assigned thereto a processing destination identifier indicating a subsequent processing destination determined based on information included in the data; and

a switch which provides the data to the subsequent processing destination based on the processing destination identifier.

2. The data processing circuit as claimed in claim 1 wherein the predetermined processing comprises traffic processing.

3. The data processing circuit as claimed in claim 1, further comprising a line interface which provides the switch with the data having assigned thereto a processing destination identifier indicating the data processor which is a first processing destination.

4. The data processing circuit as claimed in claim 1, further comprising a mother board which mounts the switch and a connector which connects the switch and the data processor, and

a controller which manages a configuration state of the data processor and notifies the configuration state to the data processor.

5. The data processing circuit as claimed in claim 4, further comprising a memory which preliminarily stores the configuration state of the data processor provided to the controller.

6. The data processing circuit as claimed in claim 5, further comprising an input portion inputting the configuration state to the memory.

7. The data processing circuit as claimed in claim 4 wherein the data processor has data processing identifier information indicating its data processing content, and

the controller recognizes the configuration state by reading the data processing identifier information.

8. The data processing circuit as claimed in claim 1 wherein the

data processor has data processing identifier information which indicates its data processing content, and

each data processor mutually exchanges data processing identifier information of other data processors.

9. The data processing circuit as claimed in claim 1 wherein the switch is provided with a queue temporarily holding data at a preceding stage of an input port or a subsequent stage of an output port.

10. A data processing circuit comprising:

a processing destination identifier assigning portion which assigns, to data, processing destination identifiers indicating all data processing procedures determined by information included in the data;

a switch which provides the data to a subsequent processing destination based on the processing destination identifiers, and

a data processor which returns the data to the switch after performing predetermined processing to the data received from the switch.

11. The data processing circuit as claimed in claim 10 wherein the data processor deletes a processing destination identifier indicating its own processor.

12. The data processing circuit as claimed in claim 10 wherein the switch deletes a processing destination identifier of the subsequent processing destination.

13. The data processing circuit as claimed in claim 10 wherein the predetermined processing comprises traffic processing.

14. The data processing circuit as claimed in claim 10, further comprising a mother board which mounts the processing destination identifier assigning portion, the switch, and a connector which connects the switch and the data processor, and

a controller which manages a configuration state of the data processor and notifies the configuration state to the processing

destination identifier assigning portion.

15. The data processing circuit as claimed in claim 14, further comprising a memory which stores the configuration state of the data processor provided to the controller.

16. The data processing circuit as claimed in claim 15, further comprising an input portion inputting the configuration state to the memory.

17. The data processing circuit as claimed in claim 14 wherein the data processor has data processing identifier information indicating its processing content, and

the processing destination identifier assigning portion reads the data processing identifier information.

18. The data processing circuit as claimed in claim 10 wherein the switch is provided with a queue temporarily holding data at a preceding stage of an input port or a subsequent stage of an output port.